Electronic and Signal Processing Resit

Prof. Dr. E. Chicca

Resit - July 1^{st} 2022

Information

Welcome to the Electronics and Signal Processing resit.
How to write your solution
Please use a **pen** and not a pencil. Make sure your **hand writing** is understandable by others. **Drawings** do not need to be beautiful/perfect but it is important that they are easy to understand and there are no ambiguities (e.g. a gate which could be an OR or an AND, but it is not clear which one it is from the drawing and there is no label). Each **solution** has to be justified and **the logical and mathematical steps to get there have to be explicitly written down**, only providing the final outcome will lead to zero points. On **every page** please indicate which problem you are working on. If you separate the pages please indicate your name and student ID on **every page**.

Problem 1 (14 points)

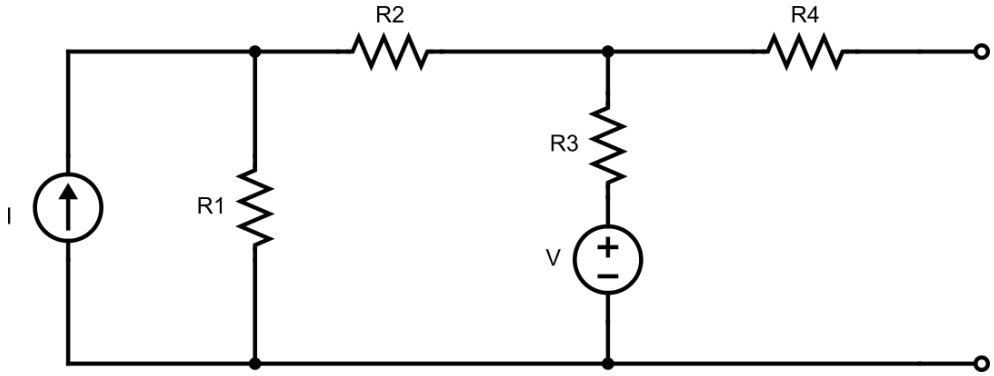


FIGURE 1: Resistor network.

Consider the circuit in Figure 1. Assume **ideal** components and the following **parameters**: $R_1 = R_2 = 1k\Omega$, $R_3 = R_4 = 2k\Omega$, $V = 12\text{V}$, $I = 6\text{mA}$

(a) (2 points) Clearly state the Norton theorem.

(b) (4 points) Determine the equivalent resistance R_{eq} seen between the output pins.

(c) (4 points) Determine the Norton equivalent current I_{sc} using the superposition principle.

(d) (4 points) Consider now a $10k\Omega$ load resistor placed between the output pins. What will be the voltage over this resistor? Before calculating, draw the equivalent circuit and write the general equation for the voltage across the load.

Problem 1 - Solution [14]

Point a [2]

Norton Theorem: Any linear electric network can be replaced by an equivalent circuit containing a single independent current source I_{No} and parallel resistance R_{No}. The theorem is applied to the network after shorting the load between two arbitrary terminals A and B. The equivalent current I_{No} is the current found between the terminals A and B. The equivalent resistor R_{No} is the resistance between the terminals A-B calculated after replacing all voltage sources with a short circuit and all current sources with an open circuit (i.e., replace each source with its ideal internal resistance).

Point b [4]

In order to find R_{eq} we replace the voltage & current sources with their internal resistances, that are zero & infinite respectively. Thus, replace the current source with an open circuit, and the voltage source with a closed circuit, allowing us to redraw the circuit as shown in Figure 2, giving:

$R_1 = R_2 = 1\,\text{k}\Omega$, $R_3 = R_4 = 2\,\text{k}\Omega$

$$R_{eq} = R_4 + (R_1 + R_2)//R_3 = R_4 + \left(\frac{1}{R_1 + R_2} + \frac{1}{R_3}\right)^{-1} = R_4 + \left(\frac{R_3(R_1 + R_2)}{R_1 + R_2 + R_3}\right) = \underline{\underline{3\,\text{k}\Omega}}$$

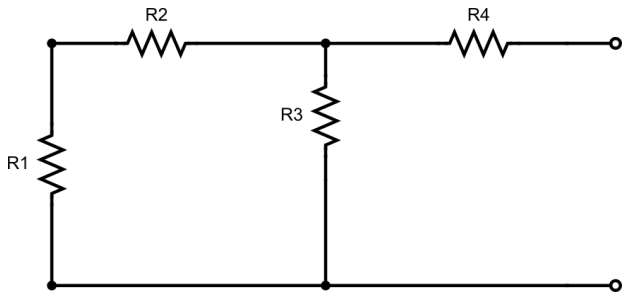


FIGURE 2: Norton equivalent circuit: finding R_{eq}

Point c [4]

The short-circuit current can be calculated using the superposition principle, studying the circuit with only one source at a time. First, keeping only the current source ignoring the voltage source, the short-circuited circuit can be redrawn (see Fig. 3). Then, we keep only the voltage source and ignoring the current source, the short-circuit circuit becomes that in Fig. 4.

Case 1: Current source only

To find the short-circuit current $I_{SC,1}$, we can start by finding I_2, which will once again branch off to give $I_{SC,1}$.

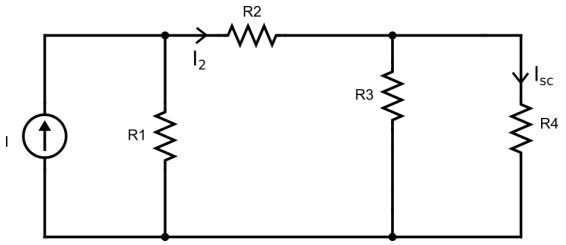


FIGURE 3: Using Norton equivalent circuit and superposition to find I_{SC} for only the current source

$$I_2 = I \frac{R_1}{\underbrace{R_1}_{\text{current through } R_1} + \underbrace{R_2 + R_3//R_4}_{\text{current through rest}}} \implies I_{SC,1} = I_2 \frac{R_3}{R_3 + R_4} = \left(\frac{I\, R_1}{R_1 + R_2 + R_3//R_4} \right) \frac{R_3}{R_3 + R_4}$$

each branch current is inversely proportional to its resistance/impedance

$$I_{SC,1} = \frac{IR_1}{R_1 + R_2 + \dfrac{R_3 R_4}{R_3 + R_4}} \frac{R_3}{R_3 + R_4} = \frac{IR_1}{\dfrac{(R_1 + R_2)(R_3 + R_4) + R_3 R_4}{\cancel{R_3 + R_4}}} \frac{R_3}{\cancel{R_3 + R_4}} = \underline{1\,\text{mA}}$$

$R_1 = R_2 = 1\,\text{k}\Omega$, $R_3 = R_4 = 2\,\text{k}\Omega$, $I = 6\,\text{mA}$

Case 2: Voltage source only

To find the short-circuit current $I_{SC,2} =$, it is useful to redraw it as in figure 4. After this, we start with the total current $I_{\text{total}} = \dfrac{V}{R_3 + (R_1 + R_2)//R_4}$

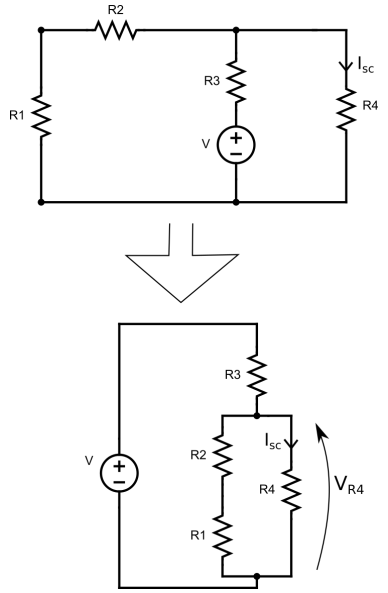


FIGURE 4: Using Norton equivalent circuit and superposition to find I_{SC} for only the voltage source

$$I_{SC,2} = I_{total} \frac{R_1 + R_2}{\underbrace{R_4}_{\text{current through } R_4 = I_{SC,2}} + \underbrace{R_1 + R_2}_{\text{current through rest}}} = \left(\frac{V}{R_3 + (R_1 + R_2)//R_4} \right) \frac{R_1 + R_2}{R_4 + (R_1 + R_2)}$$

$$I_{SC,2} = \frac{V}{R_3 + \dfrac{(R_1 + R_2)R_4}{R_1 + R_2 + R_4}} \frac{R_1 + R_2}{R_4 + (R_1 + R_2)} = \frac{V}{R_3 + \dfrac{(R_1 + R_2)R_4}{\cancel{R_1 + R_2 + R_4}}} \frac{R_1 + R_2}{\cancel{R_4 + (R_1 + R_2)}} = \underline{2\,\text{mA}}$$

$R_1 = R_2 = 1\,\text{k}\Omega$, $R_3 = R_4 = 2\,\text{k}\Omega$, $V = 12\,\text{V}$, $I_{\text{total}} = 12\,\text{V}/3\,\text{k}\Omega = 4\,\text{mA}$, $I_{\text{total}} = 4\,\text{mA}$

You could also find $I_{SC,2}$ using the voltage drop across resistor R_4 divided by its resistance. Here, we use a potential divider setup to find the voltge drop, giving

$$I_{SC,2} = \frac{V_{R_4}}{R_4} = \frac{1}{R_4} V \frac{(R_1 + R_2)//R_4}{R_3 + (R_1 + R_2)//R_4} = \underline{2\,\text{mA}}.$$

Therefore, the total short-circuit current found through the method of superposition will be

$$I_{No} = I_{SC} = I_{SC,1} + I_{SC,2} = \underline{\underline{3\,\text{mA}}}.$$

Point d [4]

In order to find the behaviour when a load resistor is placed across the output terminals, we can replace the circuit by its Norton equivalent, which is characterized by $I_{No} = I_{SC} = 3\,\text{mA}$ and $R_{No} = R_{eq} = 3\,\text{k}\Omega$. The resultant circuit is shown in Fig. 5, and we see that the voltage across the load can be found using Ohm's Law with the current source and the parallel resistors. For a load resistor $R_L = 10\,\text{k}\Omega$, the voltage drop V_L with current I_L passing through it (find using current divider) is given by:

$$V_L = I_L R_L = \left(I_{SC}\frac{R_{eq}}{R_{eq}+R_L}\right)R_L \text{ or } V_L = \frac{I_{SC}}{R_{eq}//R_L}$$

$R_{eq} = 3\,\text{k}\Omega$
$R_L = 10\,\text{k}\Omega$
$R_{eq}//R_L = \frac{30}{13}\text{k}\Omega$
$I_{SC} = 3\,\text{mA}$

Thus, the voltage across the resistor will be $V_L = \frac{9}{13}\text{mA} \cdot 10\,\text{k}\Omega \approx \underline{\underline{6.923\,\text{V}}}$.

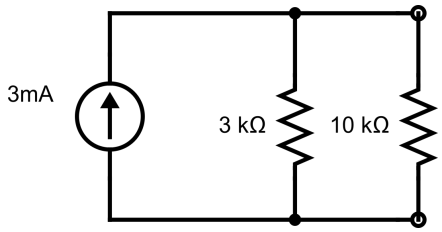


FIGURE 5: Norton equivalent circuit with load resistor R_L

Remarks

- This problem is rooted in the superposition principle and is analogous to *Top problem 2.2* with minor changes such as the voltage/current sources having exchanged places, and there are only 4 resistors in this problem as compared to the five in the Top problem.
- This builds on the notion of equivalent circuits and the effects of loading: the extent of knowledge needed is mostly limited to Ohm's law

Problem 2 (22 points)

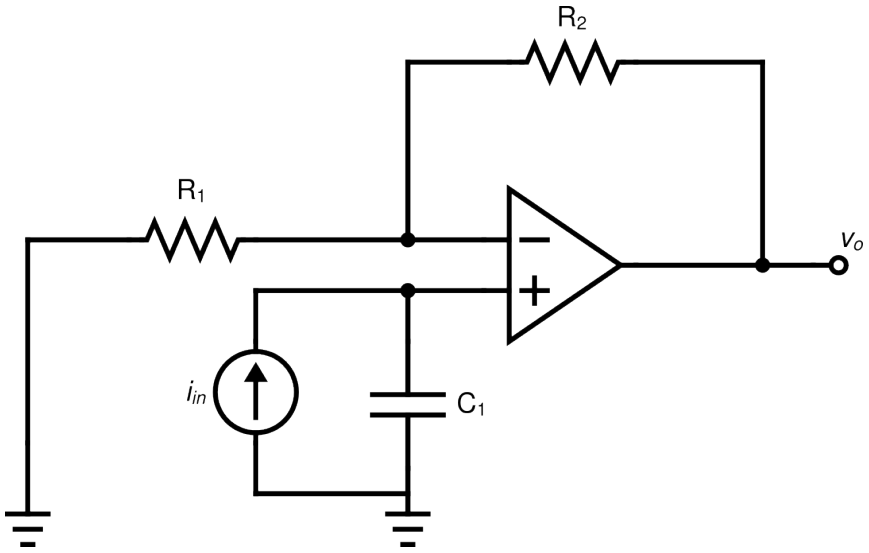


FIGURE 6: Circuit with op-amp.

Consider the circuit in Figure 6. It operates in a **sinusoidal** regime with an **ideal** opamp and **ideal** components.

(a) (18 points) Find the transfer function $H(j\omega) = \frac{v_o}{i_{\text{in}}}$ between i_{in} and v_o, depending only on R_1, R_2, C_1, and ω. Then, given that $R_1 = R_2 = 1k\Omega$, $C_1 = 1\mu$F, and $i_{in} = 2\sin(\omega_o t)$mA with $\omega_o = 1000$rads/s, find v_o as a function of time t.

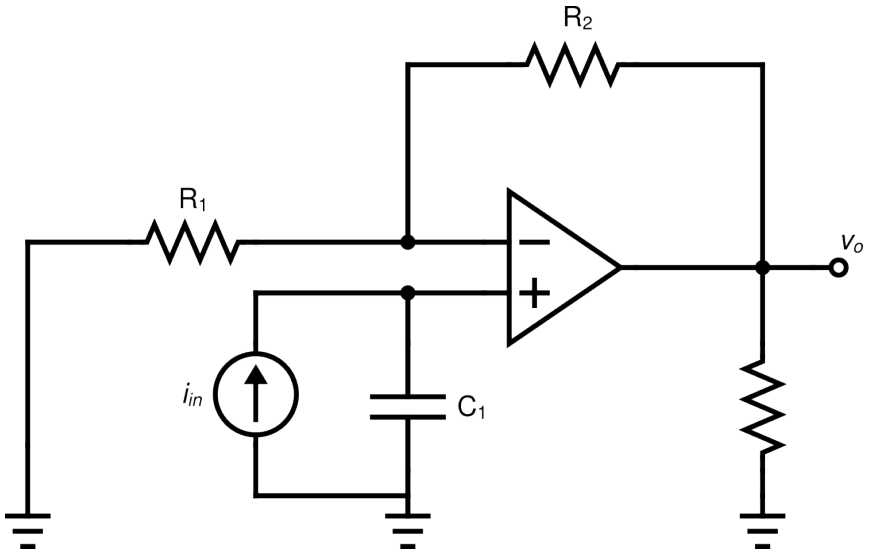


FIGURE 7: Circuit with extra resistor.

(b) (4 points) We add a resistor to the circuit as shown in figure 7. Explain, without calculating, what (if anything) this changes to the transfer function (e.g. frequency dependence, gain) and why.

Problem 2 - Solution

Point a [18]

Solution

Using a potential divider setup (see Figure 8), we can see that $v_- = v_0 \dfrac{R_1}{R_1 + R_2}$. Further, the non-inverting input to the op-amp v_+ can be found using the impedance in parallel to the current source, giving $v_+ = i_{in} Z_{C_1} = i_{in} \dfrac{1}{j\omega C_1}$.

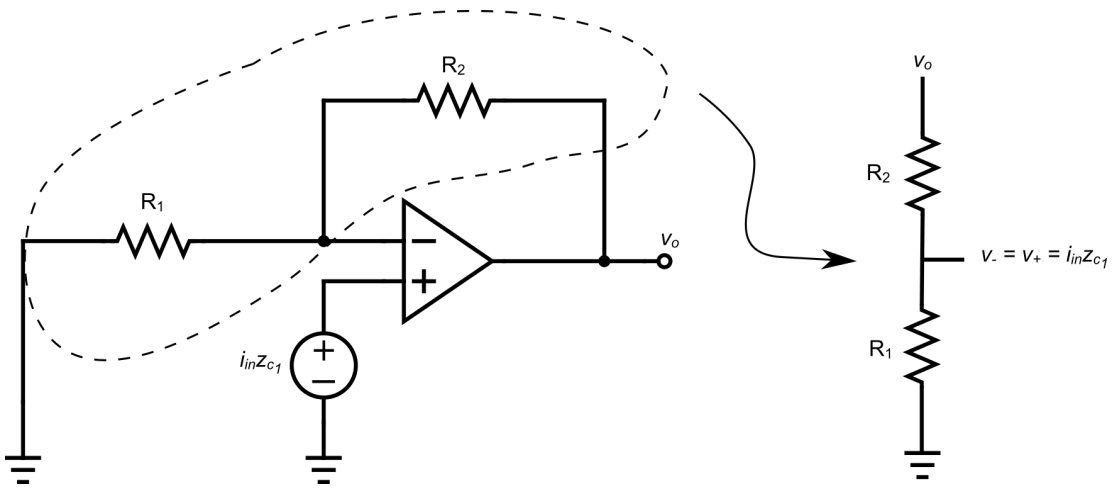


FIGURE 8: Using a potential divider to find the transfer function of the op-amp circuit

As follows from an ideal op-amp, $v_+ = v_-$ thus:

$$v_+ = v_- \implies i_{in} \frac{1}{j\omega C_1} = v_0 \frac{R_1}{R_1 + R_2} \implies v_0 = i_{in} \frac{R_1 + R_2}{R_1} \frac{1}{j\omega C_1} = i_{in} \left(1 + \frac{R_2}{R_1}\right) \frac{1}{j\omega C_1}$$

$$\boxed{\therefore H(j\omega) \equiv \frac{v_0}{i_{in}} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{j\omega C_1}} \implies v_0 = \left(1 + \frac{R_2}{R_1}\right) \frac{i_{in}}{j\omega C_1}$$

$$\because H(j\omega) \equiv \frac{v_0}{i_{in}} \implies v_0 = \left(1 + \frac{R_2}{R_1}\right) \frac{i_{in}}{j\omega C_1} = \left(1 + \frac{1\,\text{k}\Omega}{1\,\text{k}\Omega}\right) \frac{2\,\text{mA} \sin \omega_0 t}{j\omega_0 \cdot 1\,\mu\text{F}} = -j \frac{\sin \omega_0 t}{\omega_0} \frac{4\ \text{mA}}{\omega_0 1 \times 10^{-6}\,\text{F}}$$

$$\implies v_0(t) = \frac{-4000j}{\omega_0} \sin \omega_0 t\ \text{V} = -4j \sin\left(\omega_0 t - \frac{\pi}{2}\right) \text{V} \text{ for } \omega_0 = 1000\,\text{rad}\,\text{s}^{-1}$$

$$\implies \boxed{v_0(t) = 4 \sin(1000t - \tfrac{\pi}{2}) = -4 \cos(1000t) \text{V}}$$

Point b [4]

Solution

The addition of the resistor to the output of the op-amp has no influence on the potential divider setup to find v_- and thus feedback, the transfer function $H(j\omega)$ remains unchanged; this means that the op-amp will generate the same output voltage v_0 regardless of the influence of this additional resistor. In essence, the gain, the frequency, and op-amp output stay the same, due to the position of this resistor.

Remarks

- Comparable to the concepts and complexity of a range of op-amp based problems as sampled in Top problems 4–7 (similar but takes the concepts further: Top problems 8–10).

Problem 3 (18 points)

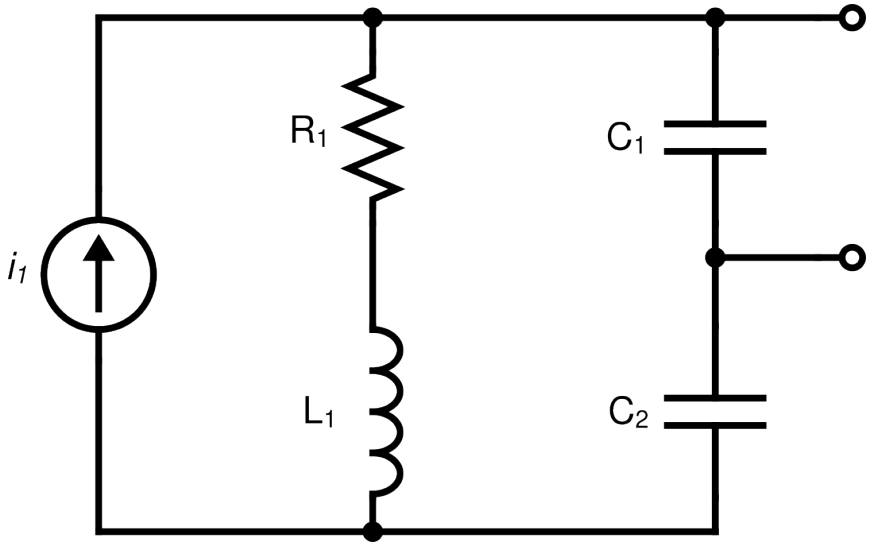


FIGURE 9: RLC circuit.

Consider the circuit in Figure 9. Assume **sinusoidal** regime, **ideal** components and the following **parameters**: $C_1 = 1$ F, $C_2 = 2$ F, $R = 1\ \Omega$, $L = 1$ H, $i_1 = I_1 \sin(\omega t)$, and $\omega = 1$ rads/s.

(a) (4 points) Write the impedance of each element (L_1,R_1,C_1, and C_2) and use the parameters provided above to express it as a complex impedance in Ohms.

(b) (10 points) Calculate the amplitude of the output voltage, V_o, at the terminals as a function of the amplitude of the input current, I_1.

(c) (4 points) What is the current through C_1 as $\omega \to 0$? What about the case $\omega \to \infty$? Explain your answer in detail.

Problem 3 - Solution

Point a [4]

Solution

The complex impedances for $R_1 = 1\,\Omega$, $L_1 = 1\,\text{H}$, $C_1 = 1\,\text{F}$, $C_2 = 2\,\text{F}$, $\omega = 1\,\text{rad}\,\text{s}^{-1}$, and $i_1 = I_1 \sin \omega t$ are as follows:

- C_1: $Z_{C_1} = \frac{1}{j\omega C_1} = \frac{1}{j} = -j\ \Omega$
- C_2: $Z_{C_2} = \frac{1}{j\omega C_2} = \frac{1}{2j} = \frac{-1}{2} j\ \Omega$
- L_1: $Z_{L_1} = j\omega L_1 = j\ \Omega$
- R_1: $Z_{R_1} = R_1 = 1\,\Omega$

Point b [10]

Solution

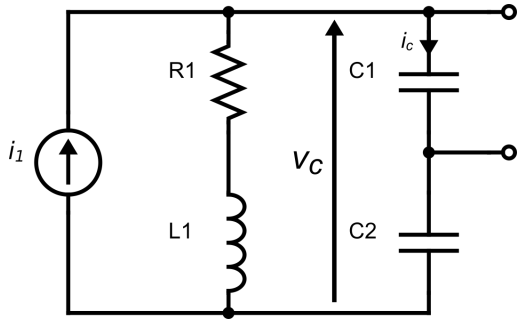


FIGURE 10: RLC circuit with the voltage across the pair of parallel connections V_x indicated

The voltage across the parallel pairs in the circuit (across R_1 and L_1, and across C_1 and C_2) can be found by Ohm's law — this will use the current from the source i_1, and the circuit's (input) impedance over the parallel pairs, which is $(Z_{R_1} + Z_{L_1})//(Z_{C_1} + Z_{C_2})$.

$$v_C = i_1(Z_{R_1} + Z_{L_1}) \;//\; (Z_{C_1} + Z_{C_2}) = i_1\ [(1+j)\ \Omega \;//\; (-3/2 j\ \Omega)] = i_1 \left[\frac{1}{1+j} + \frac{1}{-3/2 j}\right]^{-1}$$

$$= i_1 \frac{(1+j)(-3/2 j)}{(1+j)+(-3/2 j)} = i_1 \frac{3/2(1-j)}{1-1/2 j} = i_1 \frac{3(1-j)}{2-j} = 3 i_1 \frac{(1-j)(2+j)}{(2-j)(2+j)}$$

$$\therefore v_C = \underline{\underline{\frac{3\,i_1}{5}(3-j)\ \text{V}}} \quad \text{or } v_C = \frac{3/2(1-j)}{1-1/2 j} i_1$$

$R_1 = 1\,\Omega$
$L_1 = 1\,\text{H}$
$L_1 = 1\,\text{F}$
$C_1 = 2\,\text{F}$
$\omega = 1\,\text{rad}\,\text{s}^{-1}$

To find the current going to the capacitors, i_C, we use Ohm's law again, this time in the form $v_C = i_C Z_{C_1, C_2}$, giving us:

$Z_{R_1} = 1\,\Omega$
$Z_{L_1} = j\ \Omega$
$Z_{C_1} = -j\ \Omega$
$Z_{C_2} = -\frac{1}{2} j\ \Omega$

$$i_C = \frac{v_C}{Z_{C_1,C_2}} = \frac{v_C}{Z_{C_1} + Z_{C_2}} = \frac{v_C}{[1/j\omega C_1 + 1/j\omega C_2]} = j\omega v_C \frac{1}{\frac{1}{C_1} + d\frac{1}{C_2}} = j v_C \frac{1}{\frac{1}{1} + d\frac{1}{2}} = j v_C \frac{1}{3/2} = \frac{2}{3} j\ v_C$$

$$= \frac{2}{\cancel{3}} j\ \frac{\cancel{3}\,i_1}{5}(3-j) \quad \text{or } \frac{2}{\cancel{3}} j\ \frac{\cancel{3}/2(1-j)}{1-1/2 j} \implies \boxed{i_C = \frac{2 i_1}{5}(3-j) \quad \text{or } i_C = \frac{1+j}{1-1/2 j}}$$

Following this, the output voltage $v_0 = i_C Z_{C_1}$ turns out to be:

The current through the capacitors i_C can also be found using a current divider:

the current in each branch is inversely proportional to its resistance (or impedance)

$$i_C = i_1 \frac{Z_{R_1 L_1}}{Z_{R_1 L_1} + Z_{C_1 C_2}} = i_1 \frac{Z_{R_1} + Z_{L_1}}{Z_{R_1} + Z_{L_1} + Z_{C_1} + Z_{C_2}} = i_1 \frac{R_1 + j\omega L_1}{R_1 + j\left[\omega L_1 - \frac{1}{\omega}\left({}^1\!/_{C_1} + {}^1\!/_{C_2}\right)\right]}$$

Thus, once again using Ohm's law, the output voltage $v_0 = i_C Z_{C_1}$ is found to be:

$$v_0 = i_C Z_{C_1} = i_1 \frac{Z_{R_1} + Z_{L_1}}{Z_{R_1} + Z_{L_1} + Z_{C_1} + Z_{C_2}} \cdot Z_{C_1} = i_1 \frac{R_1 + j\omega L_1}{R_1 + j\omega L_1 + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2}} \frac{1}{j\omega C_1}$$

$$= -j i_1 \frac{1+j}{1 + \cancel{j} - \cancel{j} - \frac{1}{2}j} = i_1 \frac{1-j}{1 - \frac{1}{2}j} = i_1 \frac{\frac{1}{2} - \frac{3}{2}j}{1 + \frac{1}{2}j^2} = \frac{4i_1}{5}\left(\frac{3}{2} - \frac{1}{2}j\right) \implies \boxed{v_0 = \frac{2i_1}{5}(3-j)\ \text{V}}$$

The output voltage v_0 can also be found using a potential divider setup for v_C splitting between the two capacitors:

$$v_0 = v_C \frac{Z_{C_1}}{Z_{C_1} + Z_{C_2}} = v_C \frac{-j}{-j - {}^1\!/_{2j}} = v_C \frac{\cancel{-j}}{\cancel{-j}\ {}^3\!/_2} \implies \underline{\underline{v_0 = \frac{2}{3} v_C}}$$

$$v_0 = \frac{2}{3} v_C = \frac{2}{\cancel{3}} \frac{\cancel{3} i_1}{5}(3-j) \implies v_0 = \frac{2i_1}{5}(3-j)\ \text{V}$$

Through both methods, the same result is obtained, where: $\boxed{v_0 = \frac{2i_1}{5}(3-j)\ \text{V}}$

Thus, the amplitude V_0 of the output voltage v_0 in terms of the amplitude I_1 of the input current i_1 is:

$$V_0 = |v_0| = \left|\frac{2i_1}{5}(3-j)\right| = \frac{2I_1}{5}|3-j| = \frac{2I_1}{5}\sqrt{3^2 + -1^2} \implies \boxed{V_0 = \frac{2\sqrt{10}}{5} I_1 \approx 1.265 I_1}$$

Point c [4]

Solution

At $\omega \to 0$, the impedance of the capacitors tends to infinity ($Z_C \longrightarrow \infty$), causing the current through C_1 to vanish ($i_C \longrightarrow 0$). At $\omega \to \infty$, the impedance of the capacitors drops to zero ($Z_C \longrightarrow 0$), while the impedance of the inductor goes to infinity ($Z_L \longrightarrow \infty$), thus the current becomes equal to i_1 since it doesn't flow through the inductor and all of it only flows to the capacitors.

Remarks

- Behaviour of filters and a combination of RLC components can be practiced in problems such as *Top problem 4* and those of Chapters 6 and 8 in the accompanying textbook for this course, *Electronics: A Systems Approach* by Neil Storey (6^{th} edition).

Problem 4 (16 Points)

Legend:

$$A \cdot B = \text{AND}$$

$$A + B = \text{OR}$$

$$\overline{A} = \text{NOT A}$$

(a) (4 points) Fill out the **Karnaugh map** to represent the expression below and use it to **optimise** the logic needed to implement the given expression. Please extract the **reduced** logic formula out of the Karnaugh map and do not use algebraic simplifications.

$$y = (\overline{D} \cdot \overline{C} \cdot A \cdot \overline{B}) + (\overline{D} \cdot \overline{C} \cdot A \cdot B) + (D \cdot C \cdot \overline{A} \cdot \overline{B}) + (D \cdot C \cdot A \cdot \overline{B}) + (D \cdot C \cdot A \cdot B) + (\overline{D} \cdot C \cdot A \cdot \overline{B}) + (\overline{D} \cdot C \cdot A \cdot B)$$

(b) (12 points) Design a synchronous modulo 5 up-counter as shown in the state table below based on JK-flipflops. Make use of Karnaugh diagrams and obtain the correct Boolean expression for each Q, then draw the circuit.

State	Q_1	Q_2	Q_3
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0

TABLE 1: The state table for a modulo 5 up-counter

Hint: start with a modulo-8 counter and then use a reset at the right moment.

Problem 4 - Solution

Point a [4]

Solution

Karnaugh maps are ordered in Gray code to ensure that only one variable changes between adjacent cells, and each cell is filled in with a binary digit corresponding to the output based on the cell's inputs. Each of the terms in $y = (\bar{D}\cdot\bar{C}\cdot A\cdot\bar{B})+(\bar{D}\cdot\bar{C}\cdot A\cdot B)+(D\cdot C\cdot\bar{A}\cdot\bar{B})+(D\cdot C\cdot A\cdot\bar{B})+(D\cdot C\cdot A\cdot B)+(\bar{D}\cdot C\cdot A\cdot\bar{B})+(\bar{D}\cdot C\cdot A\cdot B)$ appear as '1' on the cells, the rest are zeroes.

Mark all groups of 2 (one variable reduced), 4 (two variables reduced), 8 (3 variables reduced), 16 (all variables reduced) that you can find, individual positions can be used in multiple groups. Groups can be formed over the edge. Some possible Karnaugh maps are listed on the next page. After drawing the maps, we can find the simplified expression:

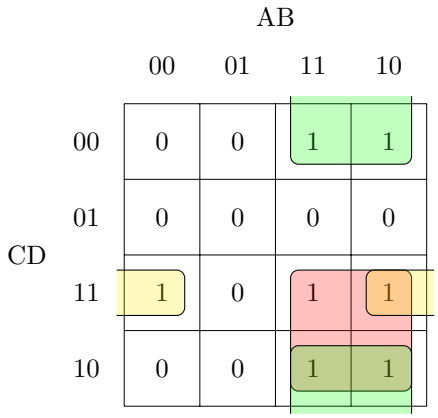
$$y = (A \cdot \overline{D}) + (\overline{B} \cdot C \cdot D) + (A \cdot C)$$

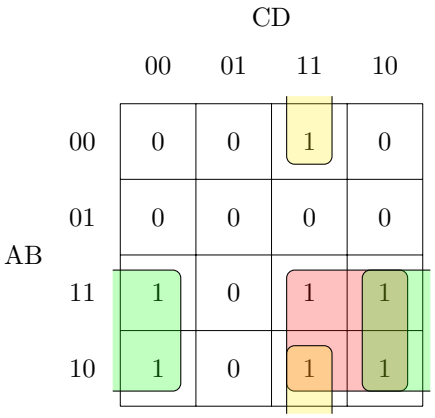
On (some of) the possible Karnaugh maps shown, the terms in y correspond to the following coloured groupings:

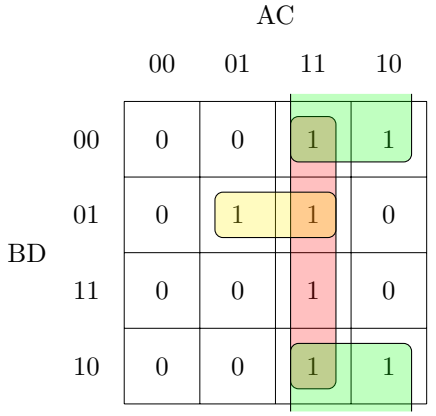
$$y = \underbrace{(A \cdot \overline{D})}_{\text{green}} + \underbrace{(\overline{B} \cdot C \cdot D)}_{\text{yellow}} + \underbrace{(A \cdot C)}_{\text{red}}$$

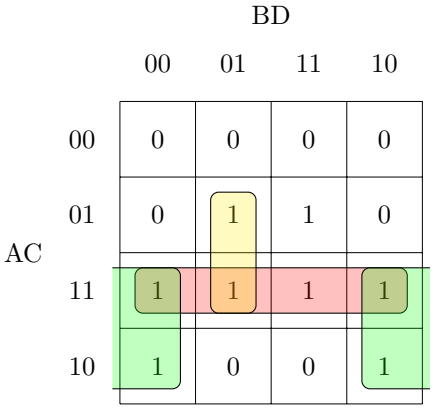
Legend:

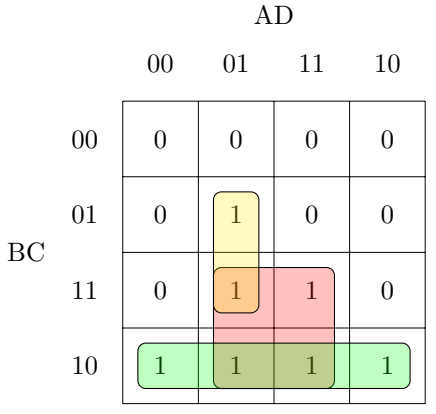
$A \cdot B$ = AND
$A + B$ = OR
$\overline{A}$ = NOT A

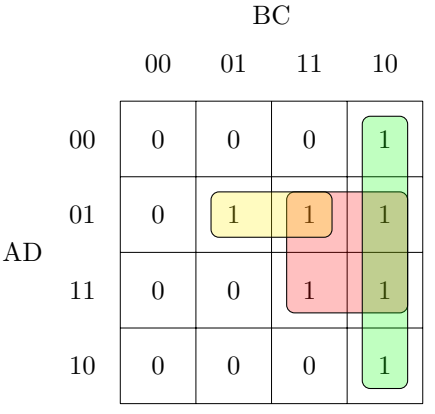

AB
00 01 11 10
CD
00 0 0 1 1
01 0 0 0 0
11 1 0 1 1
10 0 0 1 1


CD
00 01 11 10
AB
00 0 0 1 0
01 0 0 0 0
11 1 0 1 1
10 1 0 1 1


AC
00 01 11 10
BD
00 0 0 1 1
01 0 1 1 0
11 0 0 1 0
10 0 0 1 1


BD
00 01 11 10
AC
00 0 0 0 0
01 0 1 1 0
11 1 1 1 1
10 1 0 0 1


AD
00 01 11 10
BC
00 0 0 0 0
01 0 1 0 0
11 0 1 1 0
10 1 1 1 1


BC
00 01 11 10
AD
00 0 0 0 1
01 0 1 1 1
11 0 0 1 1
10 0 0 0 1

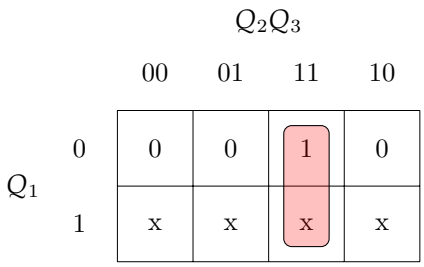
Point b [12]

Solution

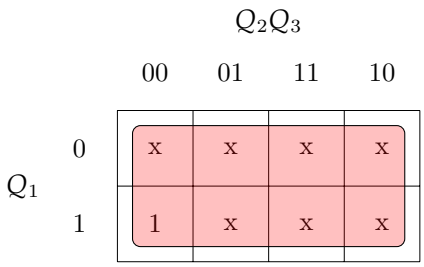
In order to design the counter, we first create the state table as shown in Table 2. From this, we can then set up the Karnaugh maps, allowing us to find the expressions, as shown below.

Current state	Next state	Q_1	Q_2	Q_3	Q_1'	Q_2'	Q_3'	J_1	K_1	J_2	K_2	J_3	K_3
0	1	0	0	0	0	0	1	0	x	0	x	1	x
1	2	0	0	1	0	1	0	0	x	1	x	x	1
2	3	0	1	0	0	1	1	0	x	x	0	1	x
3	4	0	1	1	1	0	0	1	x	x	1	x	1
4	0	1	0	0	0	0	0	x	1	0	x	0	x

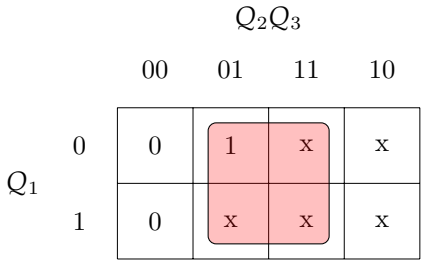
TABLE 2: State table for the modulo 5 up-counter



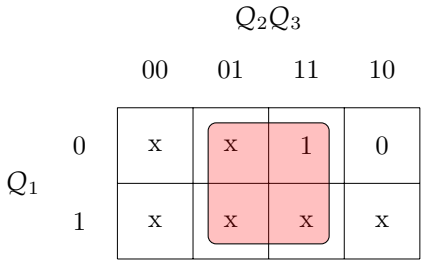
$J_1 = Q_2Q_3$



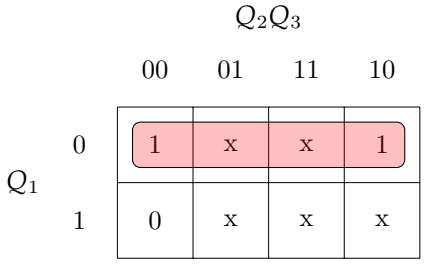
$K_1 = 1$



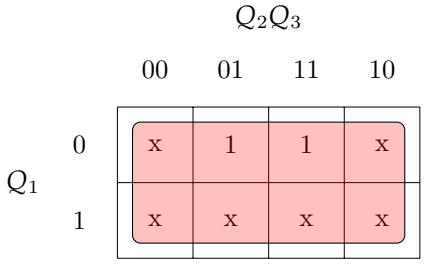
$J_2 = Q_3$



$K_2 = Q_3$



$J_3 = \overline{Q_1}$



$K_3 = 1$

After finding the simplified expressions from the Karnaugh maps, we can draw the circuit:

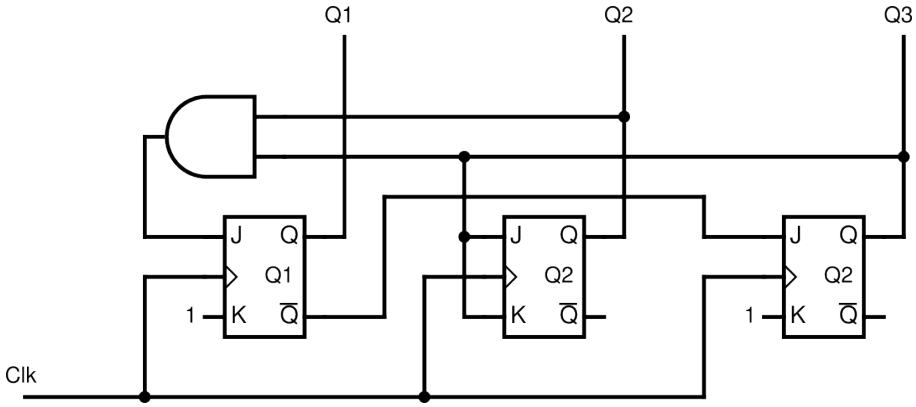


FIGURE 11: The circuit obtained for the modulo-5 counter

Remarks

- The Karnaugh map for question 4(a) is comparable to the one provided in the solution of *Exercise 24.16* in the accompanying textbook (*Electronics: A Systems Approach* by Neil Storey (6^{th} edition)) - and is provided in week 6 tutorials on Nestor. The Karnaugh maps needed for *Exercises 24.23* and *24.24* (part of the tutorial assignments of week 6, see Nestor and related solutions) are somewhat more complex than this one.
- This counter design problem is a simplified version of *Top problem 12.1*, using 3 bits instead of 4.